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Experimental Investigation of Parasitic Effects in High Electron Mobility AlGaN/GaN Heterostructure Grown on Si(111) Substrate

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Abstract. AlGaN/GaN High Electron Mobility Transistors (HEMTs) with silicon (111) substrates reveal some anomalies (parasitic) like kink effect, hysteresis phenomena and degradation in saturation current on Ids-Vds and Ids-Vgs as a function of temperature. These anomalies on output characteristics changes when we vary measurement conditions (temperature, polarisation, stress...). These parasitic effects can be attributed to the presence of deep- level on the hetero-structure.

Keywords: *AlGaN/GaN; HEMT; Kink effect, hysteresis effect and Traps.*

1. Introduction

The wide variety of unique physical properties, for example, high breakdown field strength, high carrier density, high mobility, etc. of AlGaN/GaN high electron mobility transistors (HEMTs) grown on Si substrates have attracted a great interest for power electronics applications [1,2]. This is because, due to the cost advantage. In addition to that, unlike Radio Frequency devices, power switching devices do not require high-resistivity substrates, so most AlGaN/GaN on-Si wafers utilized for power switching applications employ conductive Si substrates. Therefore, the quality of the buffer layer on the conductive Si substrate plays an important role in the breakdown characteristics [3]. In the past, high-quality epitaxial growth techniques have been stabilized, and several companies have already commercialized AlGaN/GaN-on-Si wafers up to a several inches diameter [4, 5].

One of the main problems that continue to limit the performance of GaN-based devices is the presence of electronic traps in the device structure. In high electron mobility transistors (HEMTs), the parasitic charge moving in and out of the traps on the surface and/or in the bulk of the heterostructure affects the density of the two-dimensional electron gas (2DEG) in the channel, causing effects such as current collapse [5,6,11], drain lag [12,13], gate and light sensitivity [11] and transconductance frequency dispersion [7,8]. The characteristic time of the recharging process in GaN ranges between nanoseconds and seconds. As a result, the trapping effects can limit device performance even at relatively low frequencies. In addition, the thermally activated traps contribute significantly to the device low-frequency noise [9,10].

A number of works have been performed to study anomalous behaviors related to trapping effects on current-voltage [14]. The nature and location of traps determined by deep level transient spectroscopy (DLTS) measurements [15], or conductance deep level transient spectroscopy (CDLTS) measurements have been discussed [16].

The aim of this paper is to report anomalies observed on output characteristics leakage current, kink effect and distortions for drain current in saturation region of GaN based HEMTs on Si (111) substrates.

2. Materials and Methods

The layers used in the present study were grown on sapphire and silicium substrates by metal organic chemical vapor deposition (MOCVD). The epilayer consists of 100 nm AlN buffer, 1 mm undoped GaN, and a 20 nm $Al_{0.2}GaN_{0.8}$ barrier layer. Ohmic contacts were formed by rapid thermal annealing of evaporated Ti/Al/Ni/Au (120/2000/100/1000 A°) at 860 8C for 30 s in N_2 ambient. A pre-treatment of the ohmic contact area using SiCl4 plasma in a RIE system was performed prior to Ti/Al/Ni/Au metallization. Using on-wafer transfer length measurement patterns, the ohmic contact resistance was measured to be 0.25 Ωmm. Pt/Au (100/1000 A°)

metals were evaporated for gate metallization. Overlay metallization on the ohmic contacts and measurement pads was also deposited during gate formation. Finally, a 120 nm thick passivation layer of silicon nitride was deposited using a PECVD system. The silicon nitride was then patterned and etched using SF6 plasma in an ICP-RIE system to open windows to the contact pads. The devices had a gate width of 100 mm and a source-drain spacing of 2 mm. The dc characterization Id(Vds,Vgs) has been performed using a HP 4156 SMU (Source Measurement Units) for Vds, Vgs supply and Id measurement together. The DC characteristics are measured in one sequence without delay between two Id–Vds measurements. For the measurement of the direct transconductance G_m and output conductance G_{ds}, a double power supply (HM8142) was used for the bias of the gate and the drain. The small sinusoidal excitation signal to the drain (or the gate for transconductance measurements) is provided by a gain and phase impedance analyzer (HP4194) with a frequency range extending between 10 Hz and 40 MHz. The amplitude of the ac excitation was fixed to 50 mV. The measurements were made between 77 and 550 K using a nitrogen cooled cryostat.

3.. Device characteristics and discussion

Drain-source current voltage (I_{ds}-V_{ds}-T) measurements as a function of gate voltage and temperature have been performed. Output characteristics registered at different temperatures show a number of parasitic effects such as kink effect, collapse effect, and hysteresis phenomena may limit the performance of HEMT transistors expected on AlGaN/GaN on sapphire substrates

The output characteristics Ids–Vds have been measured first for HEMT with Si substrate. The gate negative voltage Vgs was increased in order to pinch-off the channel. Immediately after, the measurement is done again; we observed a small decrease of the drain current for the second measurements. An example of this degradation of drain current at 250K, 300K and 250K is shown in Fig. 1 , Fig.2 and Fig. 3

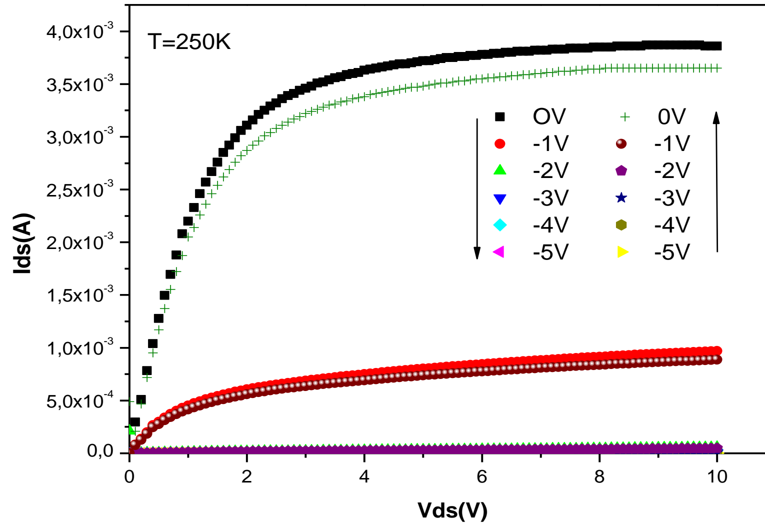


Figure.1 Drain- source current Ids versus drain- source voltage Vds of AlGaN/GaN-on-Si: measured at at T =250 K, the gate bias has been first increased from 0 to -5 V and then decreased from -5 to 0.

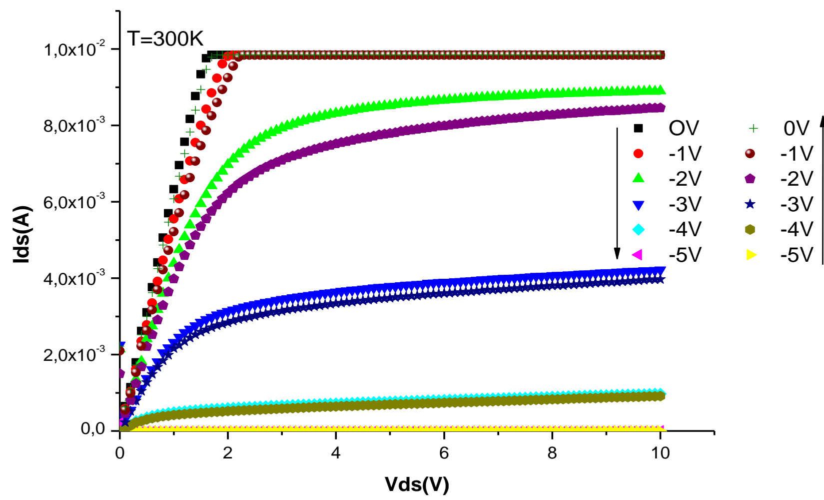


Figure-2: Drain- source current Ids versus drain- source voltage Vds of AlGaN/GaN-on-Si: measured at T=300K, the gate bias has been first increased from 0 to -5 V and then decreased from -5 to 0 V.

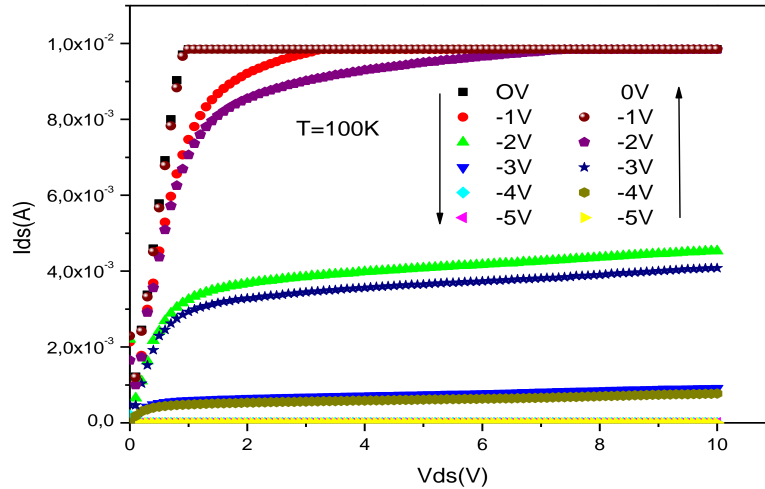
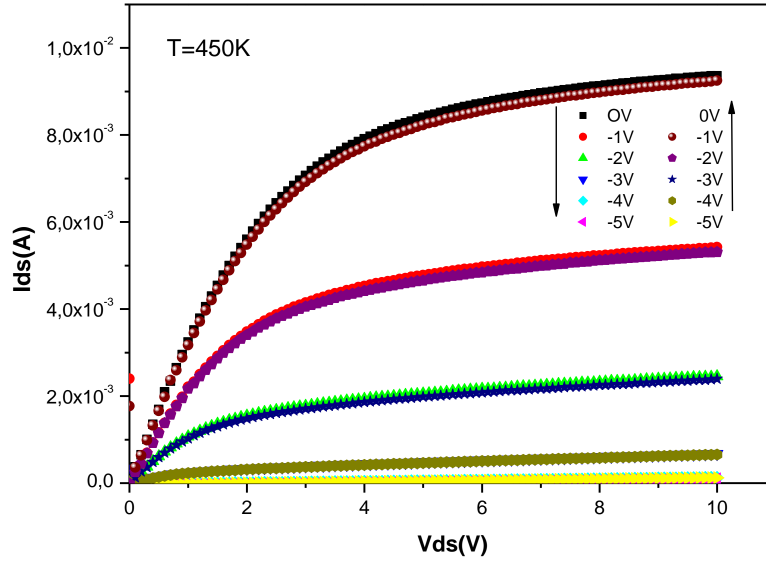


Figure.3: Drain- source current Ids versus drain- source voltage Vds of AlGaN/GaN-on-Si: measured at T=100K, the gate bias has been first increased from 0 to -5 V and then decreased from -5 to 0 V

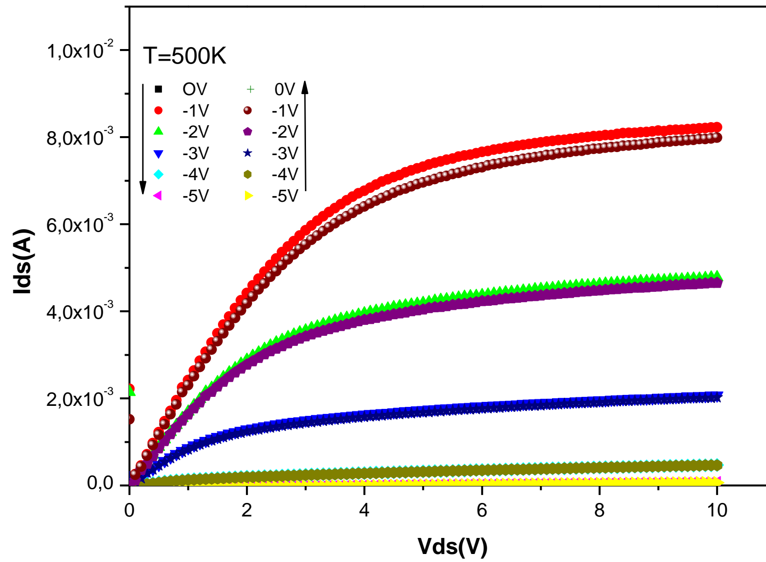
At 300 K, for high negative gate voltage (Vgs) the drain Id current changes dramatically between the two consecutive measurements. For lower value of Vgs, the effect is more intense. We have reproduced the same measurements on the same sample for higher temperature (450 K, 500K). We observed that drain current degradation gets progressively reduced, and it has almost disappeared as shown in Fig. 4 and Fig 5.

The first anomaly observed on Ids - Vds characteristics is called “Kink effect”, it consists of a sharp increase in the drain–source current at a particular drain–source voltage (Vds =V_{Kink}). This increase in drain–source current induces an increase in the drain–source output conductance (*G*ds). This effect is observed at low temperatures and starts to appear from 100 K as shown in Fig. 4. Increasing temperature, Kink effect disappears and Ids – Vds characteristics show standard variation standard without anomalies (Fig. 4). It is clear visible a reduction of Ids and an enhancement of the Kink effect when the temperature decreases down to 100 K.

This important anomaly in the I_{ds}-V_{ds} characteristics behavior is the kink effect. Some studies have established a link between the kink effect and impact ionization phenomena [17], while other studies have correlated this effect with the presence of traps in the structure.



Figures.4 Drain- source current Ids versus drain- source voltage Vds of AlGaN/GaN-on-Si: measured at T =450 K, the gate bias has been first increased from 0 to -5 V and then decreased from -5 to 0 V.



Figures.5: Drain- source current Ids versus drain0 source voltage Vds of AlGaN/GaN-on-Si): measured at T=500, the gate bias has been first increased from 0 to -5 V and then decreased from -5 to 0 V.

At biases higher than a certain critical field, a significant number of carriers injected into the barrier region have enough energy to de-trap the electrons, causing an increase in the 2DEG carrier density due to the increase of positive charge in the AlGaN layer.

A possible explanation for drain current degradation effect can be the presence of electron traps located near the conduction channel. Indeed, when a high drain voltage (10 V) is applied, the buffer layer/active layer p/n junction is highly reverse biased. Then the p-type buffer layer can be fully depleted and, because of the high electric field, electron can be injected into the substrate. This may result in a negatively charged depleted region in the substrate or the buffer near the buffer/substrate interface and consequently in the symmetric building of the depleted positive space charge region within the lower part of the channel. The negative space charge acts as a parasitic gate resulting in a drain current decrease. Indeed, for lower negative Vgs, the current flows nearer to the active layer/buffer interface and it is therefore more sensitive to the backgating influence. The reduction of the drain current degradation effect with temperature is explained by thermal evacuation of the traps.

A second parasitic effect, known as current collapse, is shown on the I_{ds}-V_{ds} output characteristics. It is more pronounced for high gate voltage, when the current flows near the substrate and for low temperatures. Gassoumi et al. [16] supposed that current collapse could occur due to the slow response of deep levels in the buffer layer, and it is more pronounced when the drain voltage V_{ds} is lowered from a higher voltage during turn-on, because the trapping effect becomes more significant.

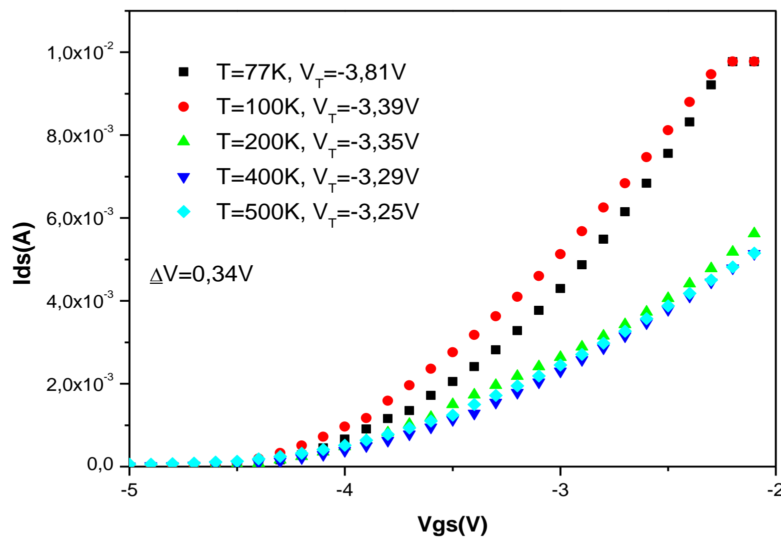
Current collapse is a trap-related phenomenon that severely limits the output power of FETs, and has been observed in nitride-based $Al_xGa_{1-x}N$/GaN heterostructure HEMT's. As reported by Mosbahi et al. [15], this effect results from the trapping of hot carriers by deep centers located in regions of the device structure outside the conducting channel. The excess charge associated with the trapped carriers produces a depletion region in the conducting channel, which results in a partial pinch-off of the device and a severe degradation of the drain current characteristics. This effect can be reversed by liberating trapped carriers either thermally by emission at elevated temperatures [15]. According to this explanation, Gassoumi et al. [16] claim that current collapse is caused by the trapping of hot electrons in deep levels at the AlGaN surface. Indeed the hot carriers were injected from the conducting channel to an adjacent region of the device that contains a high concentration of deep trapping centers. The subsequent trapping of these carriers leads to the reduced drain current.

This effect is probably attributed to the presence of deep centers located near the Si substrate and can be recovered by SiN passivation .

A hysteresis phenomenon was observed on the I_{ds}-V_{ds} output characteristics. This effect consist a increasing of the gate negative voltage Vgs in order to pinch-off the channel. Immediately after, the measurement is done again; we observed a small

decrease of the drain current for the second measurements. This effect was observed at 300K, becomes more important for low gate voltage (Fig.1-2) and disappears for low and high temperatures (figures 4 and 5). A possible explanation of this degradation in current is the presence of deep levels in the barrier layer under the gate or deep levels in the interface and/or in the buffer layer, and the surface states. Gassoumi et al. showed [17], this effect can be explained as a delay of I_{ds} answer and should be attributed to trapping and detrapping of deep centers near the surface states of channel.

As a conclusion on these first investigations, the drift on drain current characteristics presented above can be explained by the presence of deep defects near the channel for HEMTs with Si substrates.



Figures.6: Drain source current Ids and gate source voltage Vgs characteristics at T= 77 K, T =100K, 400K and T = 500 K.

Another parasitic is the threshold voltage shift with temperature. As displayed in **figure 6**, the threshold voltage (defined by a linear extrapolation of the drain current versus gate voltage to zero-current) is -3.89V at 77K, -3.39 V at 300K and -3.25V at 500 K.

This shift ΔV=0.34V is thought to be caused by deep levels associated with electrically active defects in the heterostructures [18]. It is reasonable to suggest that the change in the carrier trap density is responsible for the increase of V_{th} with the increase of temperature. The carrier trapping effects were confirmed using temperature dependence leakage current characteristics [18].

A possible hypothesis about the origin of this effect is traps. Traps are thermally activated and their charge state changes when we change temperature. These traps charge and discharge carriers and act on output characteristics. From physics point of view, a variable resistance represents these traps.

The origin of the different parasitic effects in output characteristics can you investigated using the classical Deep Level Transient Spectroscopy (DLTS) or Conductance Deep Level Transient Spectroscopy (CDLTS).

4. Conclusion

To crown all, static measurements and defect analysis on AlGaN/GaN grown on Si substrate have been investigated. In fact, Current–voltage (I_{ds}-V_{ds}-T) and (I_{ds}-V_{gs}-T) characteristics show a number of anomalies (kink effect, current collapse effect and threshold voltage shift.) attributed to trap centers and deep levels responsible for trapping/detrapping phenomenon.

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الدراسة التجريبية للشوائب في الترانزستورات عالية الحركية الإلكترونية المصنعة على ركائز السيليكون ذات الاتجاه (١١١) AlGaN–GaN

مالك القسومي و ابراهيم بشري ابراهيم تمساح

قسم الفيزياء ، كلية العلوم ، جامعة القصيم ، ص. ب. ٦٦٤٤، بريدة ٥١٤٥٢ ، المملكة العربية السعودية

ملخص البحث. تناول هذا العمل تقرير عن AlGaN–GaN الترانزستورات عالية الحركية الإلكترونية (HEMTs) المصنعه على ركائز من السيليكون ذات الاتجاة (١١١). وكان الغرض من هذا البحث هو القيام ببعض القياسات الكهربائية لمعرف الشوائب التي يمكن لها التاثير على فاعلية الترانزستورات (HEMTs) AlGaN/GaN/Si. ومن القياسات الكهربية عند درجات الحرارة المختلفة تبين لنا وجود بعض الظواهر التي تقلل من خاصية هذا النوع من الترانزستور ، ومن هذه الظواهر نذكر hysteresis effect, Kink effect. وقد تم ربط هذه الظواهر الغير محبذه بوجود بعض الشوائب الناتجة من التصنيع.