Journal of Natural Sciences and Mathematics
Qassim University, Vol. 9, No. 1, pp 95-106 (January 2016/Rabi I 1437H.)

Electrically Active Defects in 4H-SiC Schottky Barrier Diodes Characterization by DLTS System

Malek Gassoumi*[a,b]

[a]Department of Physics, College of Science, Qassim University, Buraidah 51452, Saudi Arabia.

[b]University of Monastir, Laboratory of Micro-Optoelectronics and Nanostructures,

Monastir 5000, Tunisia

Email: malek.gassoumi@gmail.com & M.Gassoumi@qu.edu.sa

Abstract. Ti/Pt/Au 4H-SiC Schottky barrier diode (SBD) has been characterized by the capacitance–voltage (C–V) technique as a function of temperature (40–310 K). The barrier height (BH) was determined as 2.45eV at the temperature of 300 K and frequency of 50 kHz from C–V measurements, respectively. Deep level transient spectroscopy (DLTS) has been used to investigate deep levels in Ti/Pt/Au 4H-SiC SBD. The five electron trap centers to be present at temperatures 251, 223, 183, 127, and 98K have been realized. The origin of these defects has been decided to be intrinsic nature and it has been found the correlation between C–V and DLTS measurements quite interesting.

Keywords: *4H-SiC Schottky barrier diode (SBD);; C-V-T measurements;; Defects DLTS.*

1. Introduction

Silicon carbide (SiC) is still one of the most attractive wide band-gap materials having many applications in the field of microelectronics and optoelectronics. The tremendous properties of SiC based semiconductor electronic devices, such as large breakdown electric field, high electron mobility and saturation electron velocity, high thermal conductivity together with good thermal stability render this material suitable for use in high temperature, high-power, and/or high-radiation conditions under which the conventional semiconductors (Si, GaAs) cannot work properly **[1]**.

Owing to its outstanding properties, it has been used to fabricate high-power, high-temperature, and high-speed devices. Ion implantation is a key process for the fabrication of semiconductor devices. For SiC materials, ion implantation of dopants has been recognized as a crucial means of selective area doping, because the thermal diffusion rates of most dopants are very slow in SiC at temperatures lower than 1800–2000C. Ion implanted MESFETs show low cost in production, low noise, high speed **[2-7]**, and planarity without mesa etching due to the creation of the active device region by the ion-implantation technique. An ion-implanted channel of MESFETs is more controllable to form thinner and more highly doped channel layers than those fabricated with conventional epitaxial growth, so it can improve the radio frequency characteristics of MESFETs.

The Schottky contacts are very important in semiconductor devices and integrated circuits. Hence many authors have investigated the properties of SiC Schottky barrier diodes (SBDs) such as Ni, Pt/4H, 6H-SiC, Ti/4H-SiC, Co/6H-SiC, Pt/6HSiC, and their structures for high voltage power devices. Ion-implantation is often used to make guard rings for SBDs, which have lower leakage current and higher breakdown voltage **[8-14].**

The prototype SiC devices deliver excellent area normalized performance, often more than 10 times better than the theoretical power density of Si power electronics. Unfortunately, nowadays there are many observable defects present in state of the art SiC homo-epitaxial layers, which have prevented the scale-up of small area prototypes into large area prototypes capable of delivering high operating currents. In addition to the high densities of crystalline defects, such as hollow-core screw dislocations (micropipes). In particular, a micropipe defect is regarded as the most damaging "device killer" defect in SiC electronics.

For example, rectifying power devices fail at micropipe defects, leading to undesired localized current flow through micropipes at electric fields far below the critical reverse-breakdown field of defect-free SiC. Over the last decade, significant efforts by SiC material vendors have succeeded in reducing micropipe densities by over a 100-fold, resulting in higher device operating currents. However, there are still very high densities of other less harmful dislocation defects, which are believed to be responsible for a variety of non-ideal device characteristics that have hindered the reproducibility and commercialization of some SiC electronic devices **[18, 19].** In this paper, we used deep level transient spectroscopy (DLTS) [20] to investigate

the electrical properties of deep levels related to defects identified in commercially available SiC Schottky barrier.

2. Experiments

The MESFETs 4H-SiC studied in this work were obtained from THALES Research and Technology (TRT) in Orsay (France) using the same fabrication process for all the transistors. The epitaxial layer structures were prepared by CVD on semi-insulating substrates supplied by CREE. The layer stack consists in three layers: a P-type buffer layer with a thickness of 0.3 μm, an N-type active layer with 0.3-0.4 μm thickness, and an N+ contact layer with a thickness and doping of 0.2 μm.

The first step consists in reactive ion etching for the channel recess. An evaporation of Ti/Pt/Au stack is realized for the gate contact. A PECVD deposited oxide layer passivates the surface. The measurements presented in this work have been realized on short test transistors with a gate length of 1μm and a gate width of 100 μm.

3. Results and discussion

3.1. Capacitance-Voltage (C-V) characteristics

The voltage dependence of the capacitance (C-V) measurement relies on the fact that the depletion region width of a semiconductor junction depends upon the applied voltage. The effective doping concentration (ND) in the active region of a Schottky diode or p-n junction can be obtained from the C-V measurement. The knowledge of effective doping concentration allows the calculation of the depletion width under certain applied bias (Equation 1.) and the determination of full depletion bias. In order to calculate the doping concentration and the built-in voltage, analysis of the data acquired from capacitance-voltage (C-V) measurements is needed.

In this study, C–V characteristics were measure at frequencies of 1MHz at temperatures ranging from 50 to 310 K.

Figure 1. Shows a C-V measurement conducted on a Schottky device. The capacitance can be seen decreasing with the increase in reverse bias because the capacitance is inversely proportional to the depletion width as is shown in Equation 1 and the depletion width (W) in a p-n junction or Schottky diode increases as reverse bias increases.

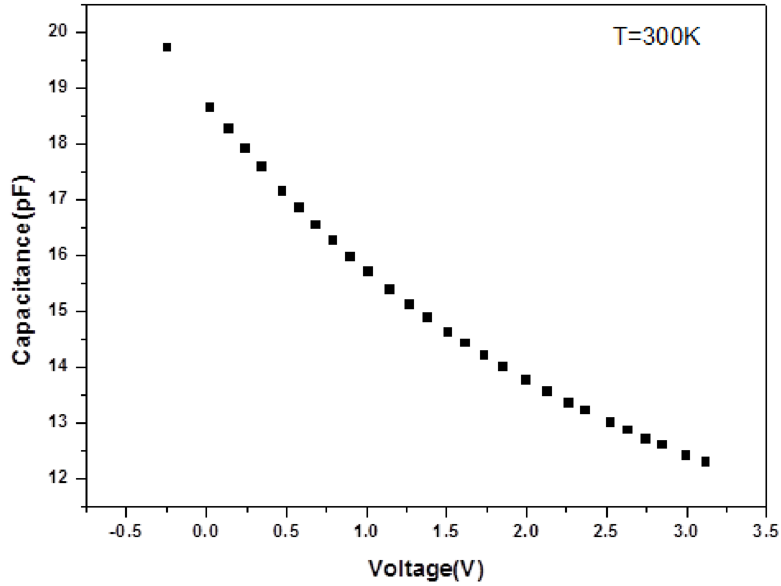

Figure 1. Capacitance-voltage (C-V) data acquired using a Schottky barrier diodes (SBDs) at T=300K

Mathematically, the capacitance of a Schottky barrier diodes (SBDs), can be expressed as [15].

$$C = \frac{\varepsilon \times \varepsilon_0 \times A}{W} = A\left[\frac{\varepsilon\varepsilon_0 N_D}{2(V_{bi}+V)}\right]^{1/2} \quad (1)$$

The variation in capacitance as a function of reverse bias is given, by:

$$\frac{1}{C^2} = \frac{2V_{bi}}{A^2 q\varepsilon\varepsilon_0 N_D} + \frac{2V}{A^2 q\varepsilon\varepsilon_0 N_D} \quad (2)$$

Which is a straight-line equation in $1/C^2$ vs. V plot (Figure 2).

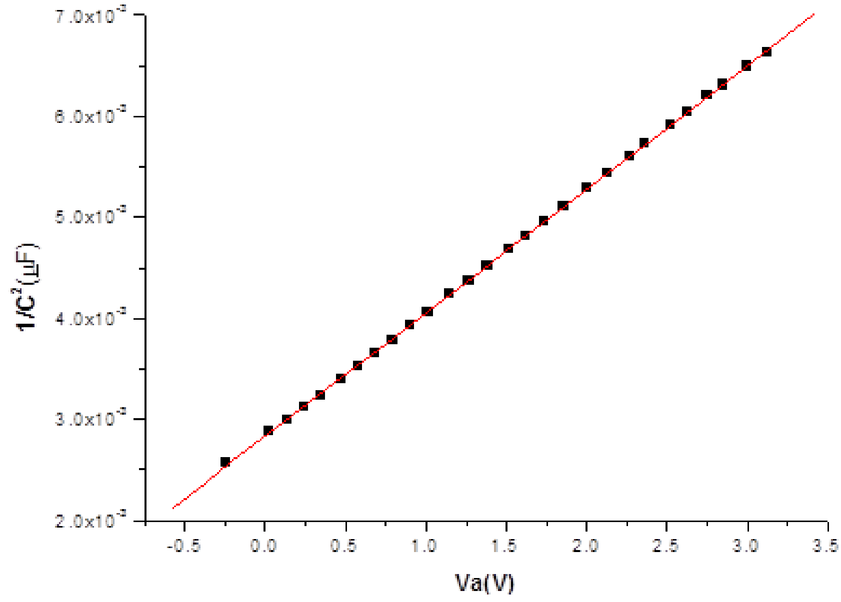

Figure 2. $1/C^2$ vs. reverse bias plot with linear fitting. Variation of $1/C^2$ as a function of reverse bias corresponding to the C-V plot shown in above. The straight line shows the linear fit of the experimental data.

The doping concentration N_D is calculated, by the following equation:

$$N_D = \frac{2}{A^2 q\varepsilon\varepsilon_0 \times slope} \qquad \textbf{(3)}$$

The value of N_D calculated from expression (3) are $N_D= 1.9\times10^{17}$ cm^3

The barrier height of SBDs can be expressed as:

$$\emptyset_B = V_{bi} + V_n + \frac{KT}{q} \qquad \textbf{(4)}$$

Where $V_n = \frac{KT}{q}\ln\left(\frac{N_c}{N_d}\right)$

Is the band gap between the bottom of the conductive band and the Fermi energy, V_{bi} is the built-in voltage of the SBDs and is the intercept on the x-axis in Fig. 2, Nc is the effective density of electrons of the conduction band, and N_d is the donor concentration. The value of $q\emptyset_B$ calculated from expression (4) are equal 2.45eV.

3.2 Defect characterization by DLTS Studies

***Principle of method*:** In a semiconductor material, defect centers could either act as an electron trap or a hole trap. These trap levels are associated with four fundamental phenomena. Electrons could be trapped by a defect level acting as an electron trap. This process is known as electron capture. Consequently, a trapped electron may get de-trapped if sufficient thermal energy is available. This process is known as electron emission. Similarly, a hole-capture process is characterized by trapping of a hole by a defect level and the hole-emission process by de-trapping of a previously captured hole. The semiconductors properties may be greatly influenced due to this charge carrier capture/emission phenomena by the defects and hence affect the efficiency of the electronic devices. Therefore, it is very important to identify and characterize the defects to understand their role in electronic and Opto-electronic device performance. The characterization would provide a deep understanding of defects in the semiconductor, which will be very helpful to enhance the efficiency of devices.

DLTS characterization

In this work, DLTS measurements were performed over a temperature ranging from 10 to 325 K, to identify and characterize the electrically active defects present in the epitaxial layers. Deep level defect parameters (i.e. activation energy, capture cross-section, and density), were calculated from the Arrhenius plots, which were obtained from the DLTS spectra at different rate windows. The observed defects in various epitaxial layers were identified and compared with the literature.

The capacitance DLTS spectra obtained for $V_r = -3V$ was employed with fill-pulse voltages $V_f = 0V$, and a time pulse $t_p= 0.5$ ms was used to fill the traps and rate windows (e_n) ranging from 20 to 200 s^{-1} are represented in Fig. 3. In order to reduce the resistance of our sample, Vgs was varied over the threshold voltage from 0V to 1.5 V. The measuring frequency of the capacitance meter varies from 20 to 200 Hz, these frequencies being small enough to avoid effects of series resistance. Moreover, to minimize the influence of the electric field on the emission rate of electron, the samples are measured at low electric field.

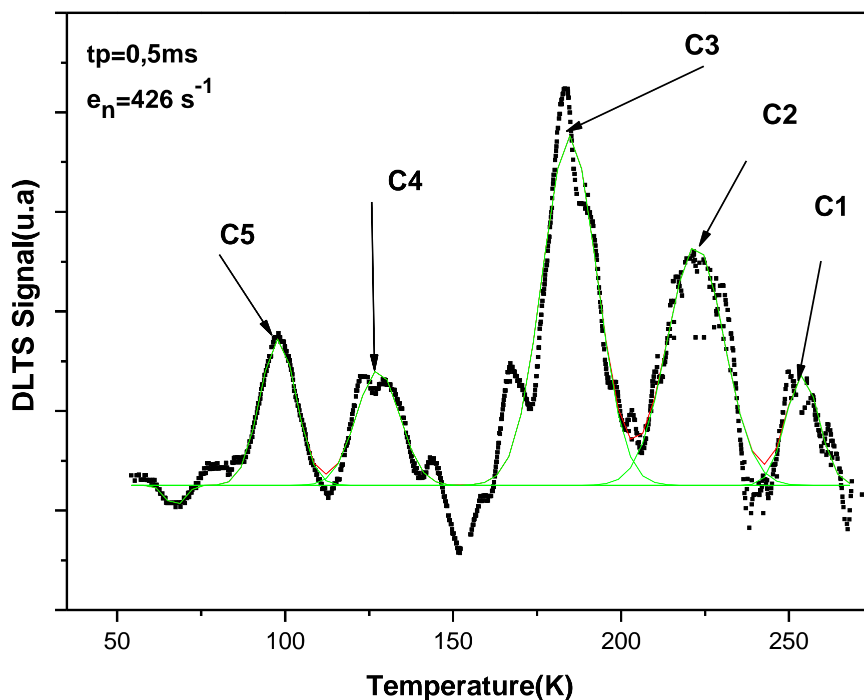

Figure 3. DLTS spectra obtained in a temperature range 50 K - 270 K

The Capacitance DLTS spectra (Fig. 3) reveal the presence of six peaks called C1, C2 C3, C4 and C5. The apparent activation energies and capture cross-sections are deduced from the Arrhenius plot of ln(T2 /en) versus 1000/T (Fig.4) of all the observed electron traps measured through Capacitance DLTS technique.

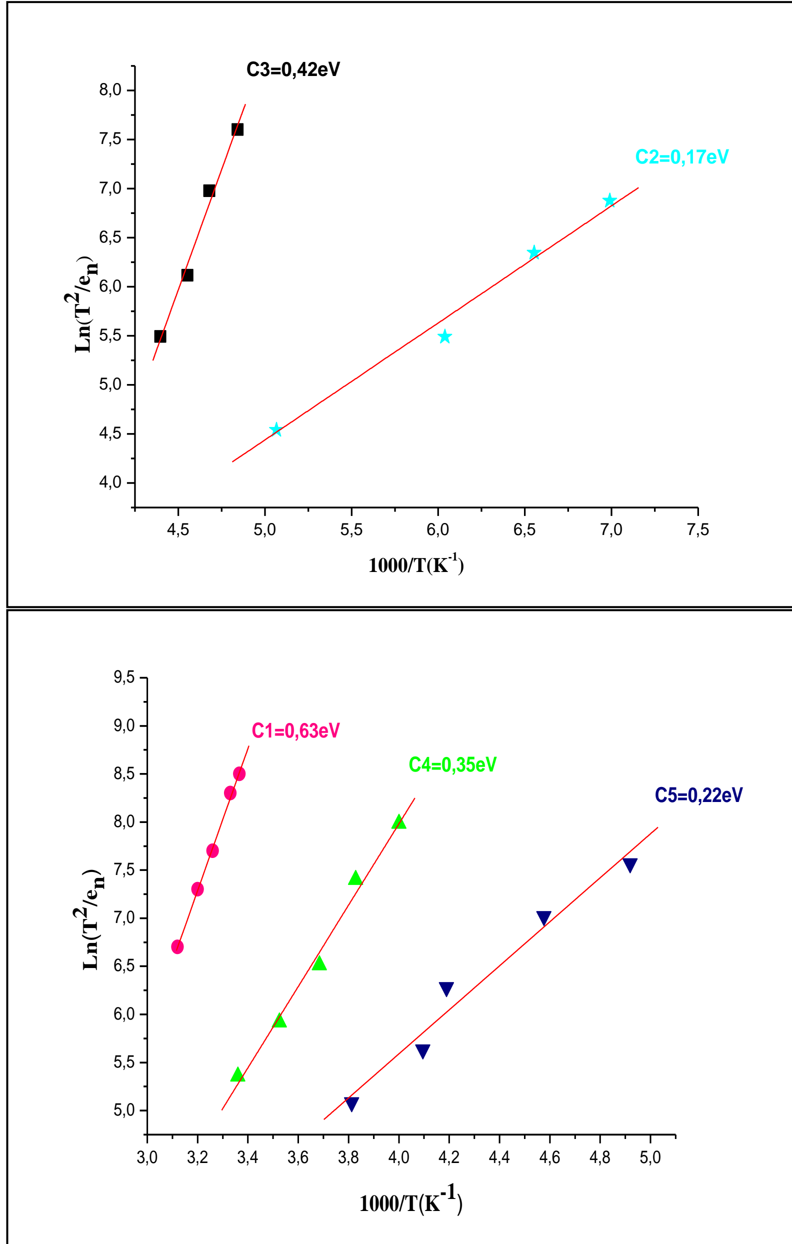

Figure 4. Arrhenius plots corresponding to the DLTS spectra of the emission time constants for the five traps C_1, C2, C3, C4 and C5.

In the following, a discussion will be evoked, concerning the origin of the observed trapping centers:

- A comparison of the obtained activation energies with those reported in the literature allows us to relate the trap center related to C1 was found to be located at 0.63 eV and capture cross section $3.4\times10^{-15}cm^2$ below the conduction band edge. Several groups have reported the presence of a similar defect level often designated as $Z_{1/2}$ [17- 21]. However, the exact microscopic structure is still unknown and several theories exist in the literature regarding the probable structure of $Z_{1/2}$ centers. As summarized by Zhang et al. [16], $Z_{1/2}$ is most likely related to defect complexes involving equal number of carbon and silicon sites.

- The trap named C_2 has an energy located at 0.43eV and a capture cross section of $9x10^{-15}$ cm^2, is mostly labeled as E_1/E_2, which can be induced by implantation or electron-irradiation. A detailed analysis of this defect level with electron irradiation and annealing by Chen et al. [28] gives rise to that its origin has been associated with primary atom displacement on the C atom of SiC sub-lattice [22].

- Regarding the C3 defect that appears with the activation energy of 0,35eV, to our knowledge this trap was only detected in this work, its origin remains an open question.

- for the C5 trap is detected have an activation energy = 0,22eV and capture cross section of $1.27\times10^{-19}cm^2$ his origin remains unknown.

- Finally the activation energy obtained from the slope of best fit line through the data points yielded the energy as shown by C_5 be 0.17eV respectively. It is well established that the transition metals introduce defects in silicon or silicon carbide, which either occupy substitutional or interstitial sites within the lattice of the material. These defects introduce shallow or deep levels within the band gap of Silicon, depending on their electronic configuration in the lattice site. Most of the transition metals like; Platinum, Copper, Nickel etc. introduce donor and acceptor deep energy levels within band gap of Silicon. For the assignment of these energy states to such defects induced by transition metals, we compared the emission rates of both the defects with published data on emission rate of transition metal related defects in Silicon Carbide in literature. The comparison reveals that emission rate data of C_5 can be compared to the emission rate data of a Ti related defects in Silicon Carbide [23].

4. Conclusion

The related deep levels in the Schottky barrier diodes 4H-SiC were directly characterized by both C-V and capacitance Deep Level Transient Spectroscopy (DLTS). Capacitance DLTS reveals cinq kinds of deep traps C1, C2, C3, C4 and C5, with an activation energy of 0.63, 0.43, 0.35, 0.22 and 0.17eV, respectively.

The analysis has lead to identify different type of defects, on the investigated wafers Schottky diodes with barrier have been realized and characterized by electrical measurements. Results show a strong influence on reverse voltage breakdown of the devices of defects. This result shows the interest of this technique for the analysis of trapping phenomena due to SiC/SiO2 interfacial defects.

References

[1] P. G. NEUDECK, SiC Technology, in: Wai-Kai Chen, Boca Raton (Eds.) The VLSI Handbook 2nd, Florida: CRC Press, (2007).

[2] M. Watanabe, D. Fukushi, H. Yano and S. Nakajima, CS Mantech Conf. p187 (2007)

[3] K. Onodera, K. Nishimura, S. Aoyama and S. Sugitani; IEEE Trans. Electron Devices 46; 310(1999).

[4] M. Feng, D. R. Scherrer, P. J. Apostolakis and J. W. Kruse; IEEE Trans. Electron Devices 43,852 (1996).

[5] C. Danzilio, Proc. Conf. GaAs Manufact. Technol. p111 (1998).

[6] M. Feng, C. L. Law, V. Eu and C. Ito; Appl. Phys. Lett. 59 (19) 1233(1991).

[7] H. Z. Tang, D Caruth and Becher. D, IEEE Electron Device Lett. 20 245(1999).

[8] Saxena. V, Su. J. N and Steckl. A. J, IEEE Trans. Electron Devices 46, 456 (1999).

[9] Malek Gassoumi, Jean-Marie Bluet, Imène Dermoul, et al. Solid-State Electronics 50 (2), 214 (2006)

[10] Lundberg. N and Ostling. M, Appl. Phys. Lett. 63 3069 (1993).

[11] Bhatnagar. P, McLarty. K and Baliga. B. J, IEEE Electron Device Lett. 13 501(1992).

[12] M. B. Karoui, R. Gharbi, N. Alzaied and M. Fathallah, Materials Science and Engineering 28 799 (2008).

[13] B. A. Hull, J. J, M. J. Sumakeris, O'Loughlin and Q. Zhang, IEEE Trans. Electron Devices 55, 1864(2008).

[14] W. L. Frey and H. Ryssel, Applied Surface Science 184, 413(2001).

[15] P. G. NEUDECK, SiC Technology, in: Wai-Kai Chen, Boca Raton (Eds.) The VLSI Handbook 2nd, Florida: CRC Press, (2007).

[16] Z. SYNOWIEC, Mater. Electron. 32 (2004).

[17] LANG D.V, J. Appl. Phys., 45, 3023 (1974).

[18] D. A. Neamen, Semiconductor Physics and Devices, Basic Principle, McGraw Hill, (2012).

[19] J. Zhang, L. Storasta, J. P. Bergman, N. T. Son and E. Janzén, Journal of Applied Physics, vol. 93, no. 8,. 4708 (2003).

[20] L. Storasta, J. P. Bergman, E. Janzen, A. Henry and J. Lu, Journal Applied Physics, vol. 96, no. 9, 4909 (2004).

[24] K. Danno and T. Kimoto, Journal of Applied Physics, vol. 100, no. 11, 113728 (2006).

[21] T. Hornos, A. Gali and B. G. Svensson, Material Science Forum, Vols. 679 - 680, 261(2011).

[26] N. Iwamoto, B. C. Johnson, N. Hoshino, M. Ito, H. Tsuchida, K. Kojima and T. Ohshima, Journal of Applied Physics, vol. 113, no. 14, pp. 143714(2013).

[22] F. Nava, A. Castaldini, A. Cavallini, P. Errani and V. Cindro, IEEE Transaction of Nuclear Science, vol. 53, no. 5, 2977(2006).

[28] X.D. Chen, C.L. Yang, M. Gong, W.K. Ge, S. Fung, C.D. Beling, J.N. Wang, M.K. Lui, C.C. Ling, Phys. Rew. Lett. 92 125504(2004).

[23] Kodigala Subba Ramaiah, I.Bhat, T.P.Chow, J.K.Kim and E.F.Schubert J. Appl. Phys.*98, 1061108 (2005).*

تحليل العيوب النشطة كهربائيا في حاجز ثنائي 4H-SiC بواسطة تقنية DLTS الشوتكي

مالك قسومي [a,b]

[a]قسم الفيزياء، كلية العلوم، جامعة القصيم، بريدة ٥١٤٥٢، المملكة العربية السعودية.

[b]فيزياء نصف الموصلة و المكونات الإلكترونية ، المنستير ٥٠٠٠، تونس

ملخص البحث. تمت تحليل الشوائب النشطة كهربائيا في حاجز ثنائي الشوتكي ديود 4H-SiC بواسطة تقنية السعة بدلالة الجهد عند درجات حرارة مختلفة من ٤٠ الى ٣١٠ كلفن. عند درجة حرارة ٣٠٠ كلفن وعند التردد ٥٠ هيرتز ومن منحنيات C-V تم قياس حاجز شوتكي ديود فوجدناه يساوي ٢,٤٥eV. ولكي نتحقق من وجود عيوب او شوائب في حاجز ثنائي الشوتكي ديود 4H-SiC استخدامنا التحليل الطيفي ذات المستوى العميق (DLTS). بهذه التقنية تم التأكد من وجود خمسة عيوب عميقة عند درجة حرارة مختلفة. أصل هذه العيوب او الشوائب تمت التأكد منها وذلك من خلال مقارنة القياسات التي قمنا بها.